UNIVERSITI TEKNOLOGI MALAYSIA

Getting Started with Quartus

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Abstract
This article introduces the Quartus software, how to find it, install it and check out the installation. Work in progress. Use at your own risk.

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1. What is Quartus

Quartus II is one of the software that can be used for a digital system design and development. It was introduced by Altera and widely used to facilitate system on IC or embedded system development. The tasks are mainly involving simulation and verification process. The designed model are simulated for functional and timing verification on Quartus II before integrated with the actual Altera devices for hardware verification.

In this tutorial, Quartus II 13.0 Web Edition will be used. This software supports both 32-bits and 64-bits operating system. Users may also use other version that meet their system requirement and the targeting Altera device.

Quartus is available in versions 2.2 through 18.0. Up until version 16, the software was called Quartus II. After Intel took over Altera in 2016, three changes were made:

- Intel branding in the software
- The Altera Quartus II is now called Intel® Quartus® Prime and Quartus II Web Edition become Quartus Prime Lite Edition
- Introduction of the Pro edition which supports the partial reconfiguration capability of the new Arria 10 FPGA

Table 2 summarizes the differences between the versions. As the version numbers get bigger, the software becomes more complex and require more computer resources. Versions 10.0 through 12 should be avoided for beginners as they require knowledge of writing *testbenches* in Verilog or VHDL. Fig. 1 summarizes the differences of the various Quartus editions.

You can view the complete information on the latest Quartus version at `https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/po/ss-quartus-comparison.pdf`.

As a rule of thumb, if your computer's processor is not suitable for number-crunching (such as Celeron/Pentium/i3/Core M) and has 4 GB RAM or less, choose version 9.1 SP 2. If you computer has an i5/i7 processor and you are working on the latest and most expensive FPGA, choose the latest version.

Table 1. *Quartus Prime editions.*

Edition	Device Support	Cost
Pro Edition	Focus on top-of-the-line devices	30 day trial
Standard Edition	Widest device support	30 day trial
Lite/Web Edition	Entry-level	Free

Table 2. *Quartus differences by simulation waveform entry.*

Quartus Version	Waveform Entry	
	Testbench	Point-and-click
3.0 - 9.1	✓	✓
10.0 - 12	✓	×
13.0 and above	✓	✓

2. Getting Quartus

This section shows the steps to download version 13.0 of Quartus II Web Edition.

The first step to downloading is to point your browser to `http://http://fpgasoftware.intel.com/?edition=lite`.

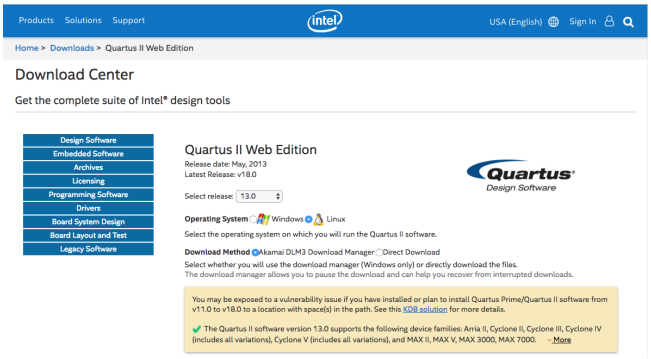


Figure 1. *Choose a version.*

You can download the full Quartus II Web Edition bundle which is 4.4GB. This will download gigabytes worth of device support which you will never use.

Download Only the Necessary Files

Since you are going to use only the CPLD chip, it is better to download only the necessary files.

1. Choose the *Individual Files* tab, and select both Quartus II and ModelSim-Altera software as shown in Fig. 2.

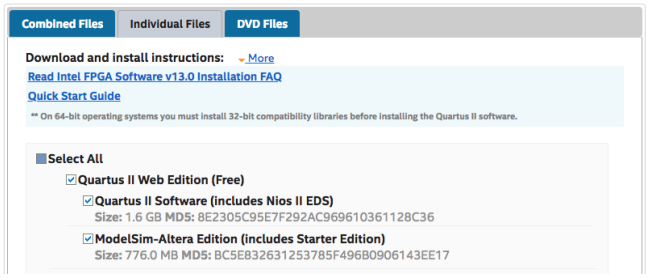


Figure 2. *Choose the design software.*

2. Choose MAX II device support. Deselect all other files.

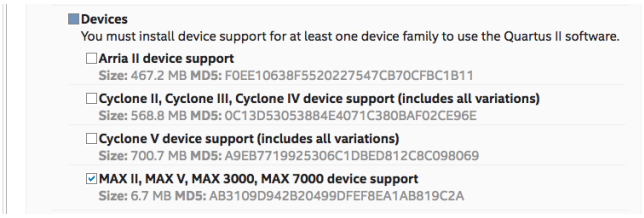


Figure 3. *Choose device support.*

4. Choose Help files if you want. The Help file can be skipped if you want to further reduce the download size.

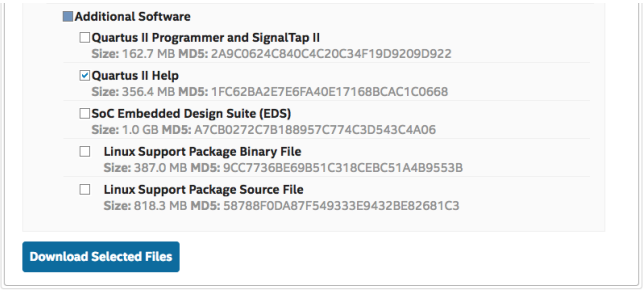


Figure 4. *Choose Programmer and Help files.*

4. Click the Download Selected Files button. You will be asked to enter your password if you have not logged in. And you may have to create an account if you have not done so. If everything is fine, you will download slightly more than 2.8 GB instead of 4.4 GB for the full package. You should have:

File	Size
QuartusSetupWeb-13.0.0.156.exe	1.64 GB
ModelSimSetup-13.0.0.156.exe	817 MB
max_web-13.0.0.156.qdz	7 MB
QuartusHelpSetup-13.0.0.156.exe	373 MB

Installing Quartus

For installation, double-click on the *QuartusLiteSetup* executable file and choose the default values.

Figure 5. *Quartus II Web Edition splash screen.*

3. Designing with Quartus

Before you can start experimenting, you should understand how Quartus does its work. Fig. 6 gives a overview. Note that Quartus software can do much more than what is shown here.

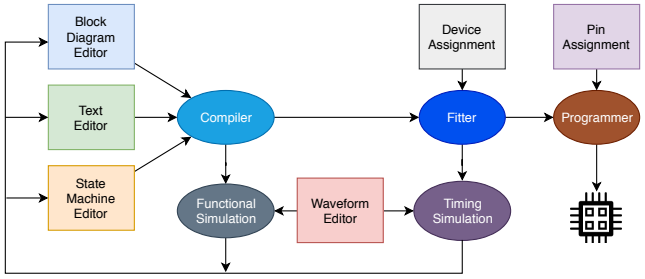


Figure 6. *Design flow using Quartus.*

The square boxes are Quartus editor or dialog boxes which you can use to enter designs or settings. They are:

- **Block diagram editor** for design entry using gates and logic blocks
- **Text editor** for design entry using hardware design language, usually Verilog
- **State machine editor** for entering a state machine
- **Waveform editor** for preparing an input waveform before simulation
- **Device assignment** is a simple dialog box to specify the target device
- **Pin assignment** is a dialog box for setting the input/output pins on the target device

The ovals are internal Quartus operations that execute commands:

- **Compiler** converts a design into a *netlist*
- **Fitter** configures the internal wiring on a target device to the netlist to obtain a *bitstream*
- **Functional simulator** performs *device-independent* simulation based on logic function only without considering the physical device aspects
- **Timing simulator** performs *device-specific* simulation which includes delay estimation. This simulation is slower than functional so it is usually done after a circuit has passed functional simulation.
- **Programmer** download the bitstream into the target device

For simple experiments with digital logic, only two boxes are used: the Block Diagram Editor and the Waveform Editor.

4. Example Design

This tutorial uses a simple circuit to check out the Quartus installation.

A combinational logic circuit shows the results for three people who vote. The three people are labeled as A, B, and C. If two out of the three people or all of them vote for a particular event, then the output of the circuit becomes HIGH. Else if only one or none of them votes, the output becomes LOW.

The truth table of the problem description are given in Table 3.

Table 3. *Voter truth table.*

Input			Output
A	B	C	V
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

There are several possible Boolean equations that can be derived. After simplifying the equation for V, we get

$$V = AB + BC + AC$$

We will now enter this circuit in Quartus and simulate its function.

5. Specifying Project Settings

1. Launch Quartus by double-clicking on the icon.

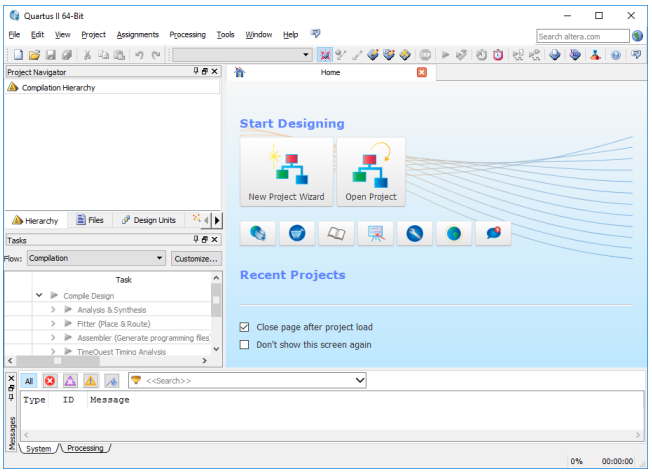


Figure 7. *Quartus II Web Edition welcome screen.*

2. Click **File ➥ New Project Wizard**. This will bring us to the introduction page.

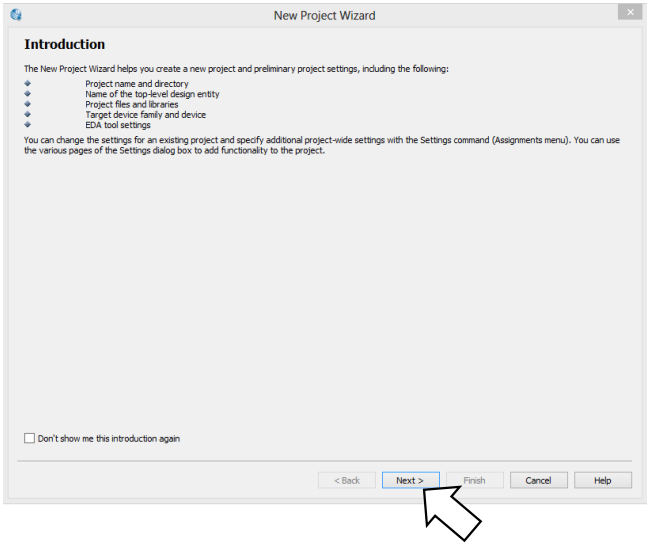


Figure 8. *New project Introduction page.*

3. Click Next >. This will bring us to page 1.

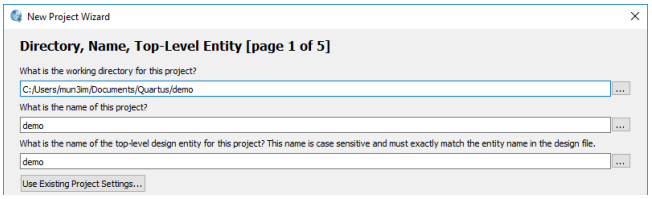


Figure 9. *Quartus II Web Edition welcome screen.*

Working directory is the location of your project files. *We strongly suggest to change the directory settings* to avoid problems if you have to reinstall Quartus and to make it easy for backing up your data. You can create a working directory at the root level of your hard disk (e.g. C:\quartusprojects) or inside your documents folder. Once you have decided on the working directory for all your Quartus projects, create a subdirectory for your current design (e.g. Voting).

Name is the name of your project. Simply use the same name at the design directory.

Top level entity specifies the master file in your design. Unless you have a specific reason, just use the project name.

4. Click Finish to go directly to the summary page. Skip all other pages for now.

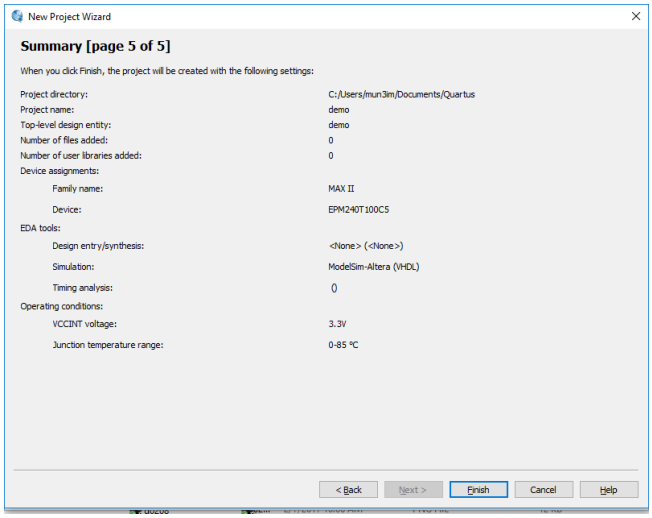


Figure 10. *Finish the Project Wizard.*

5. Click Finish. Notice the voting entity as shown in Figure 11.

The Quartus program has 4 windows:

- **Project navigator**: displays the design files in your working directory and their relationships
- **Tasks**: shows the progress of design tasks
- **Workspace**: is the area where you enter the design
- **Messages**: displays messages from the tasks e.g. compiler, fitter, simulator

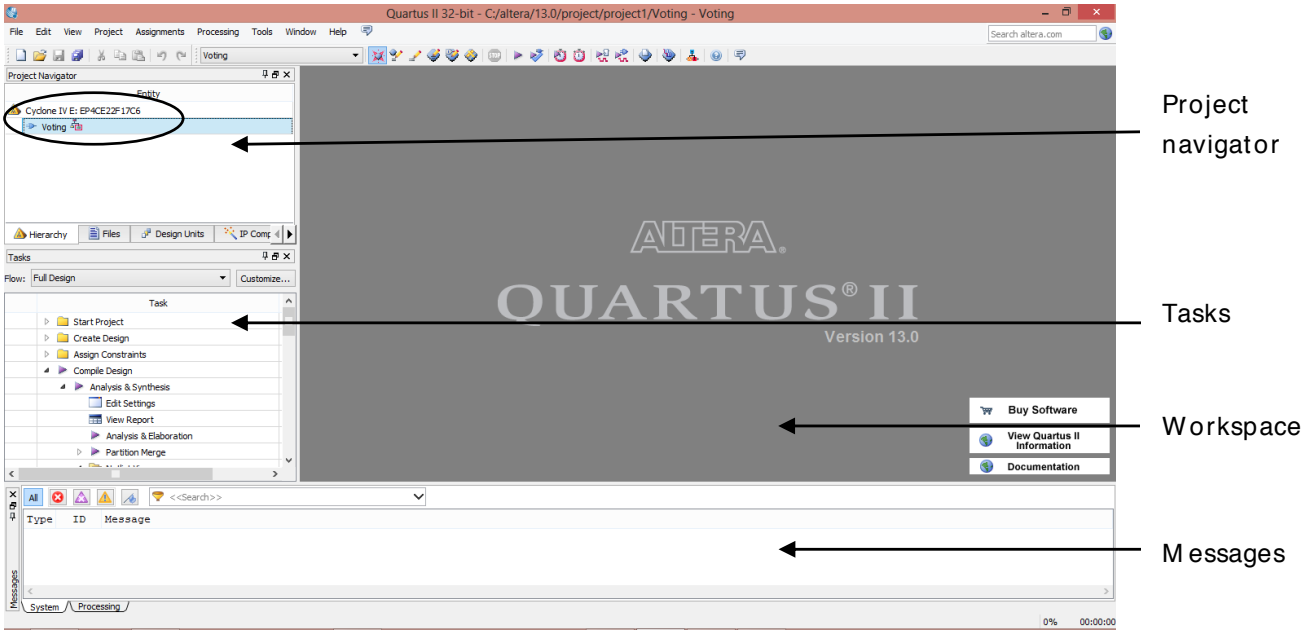
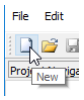


Figure 11. *Quartus layout.*

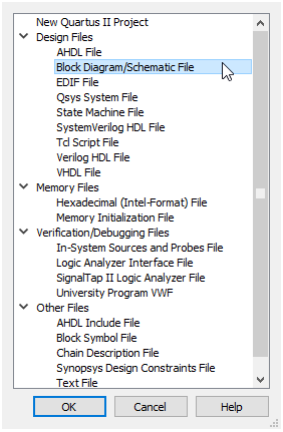
6. Schematic Entry

This section creates our design file.

1. Go to **File ➥ New** or clicking the New Document icon.



A new dialog box pops up as shown below.



2. Highlight Block Diagram/Schematic File, and click OK. The schematic entry window will appear on the working space as shown.

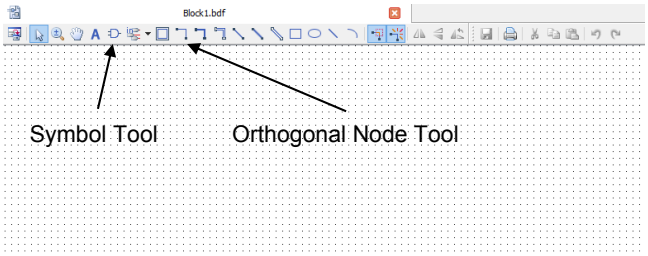


Figure 12. *Quartus schematic editor.*

3. Click Symbol Tool. A pops up dialog box will appear as shown

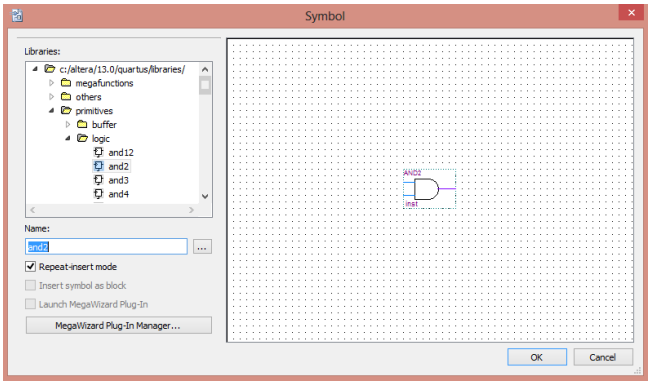


Figure 13. *Add new Symbol.*

4. Expand c:\altera\13.0\quartus\library\, expand primitive and then expand logic

5. Select and2 and then check Repeat-insert mode and then click OK.

6. Place the three (3) and2 gates as shown in Fig. 14 by clicking on the desired placing area and then press the ESC keyboard key to returns back to the normal arrow cursor

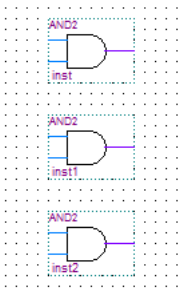


Figure 14. *Add 3 and2 gates.*

7. Repeat Step 6 to 8 for or3 gate as shown in Fig. 15.

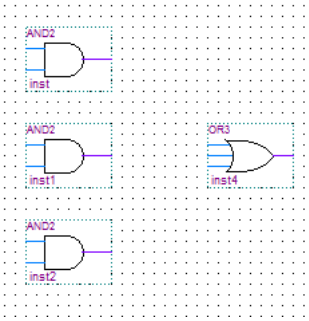


Figure 15. *Add or gate.*

8. Another way to add symbol is by clicking anywhere on the schematic editor working space. A menu box will appear. Go to Insert then click Symbol

9. Expand c:\altera\13.0\quartus\library\, expand `primitive` and then expand pin

10. Select input then click OK. By now we should have our design entry such shown in Fig. 16.

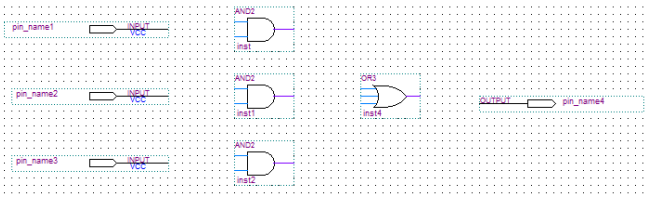


Figure 16. *All gates entered.*

11. Place the three (3) unit input pins on the workspace as describe in Step 6

12. Repeat step 8 to 11 for one output pin

13. Right-click on the top most input pin and click on Properties. We should see a pin properties pops up dialog box

14. Rename the pin name as “A”. By default, the default value will set to VCC if not, select VCC as shown in Fig. 17. Click OK.

15. Repeat the Step 13 for pin “B” and “C” and output pin “V”

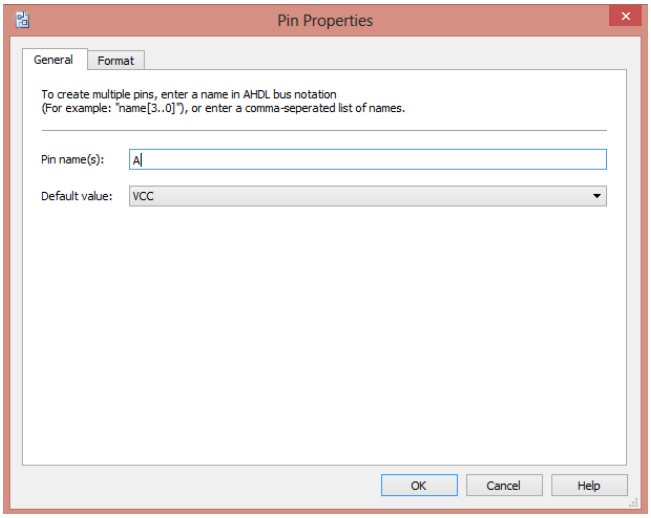


Figure 17. *Naming input pins.*

16. Select Orthogonal Node Tools on the schematic toolbars such shown in Fig. 12. Make the circuit connection for the Boolean equation. To this stage, we should see the schematics similar to Fig. 18.

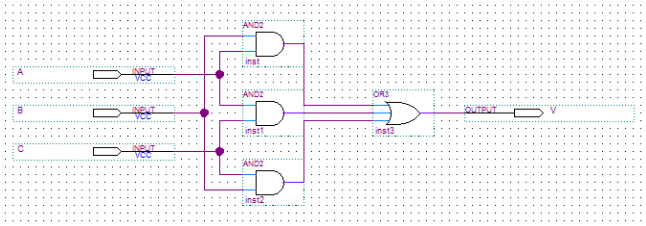


Figure 18. *Naming input pins.*

17. Go to File and click Save All

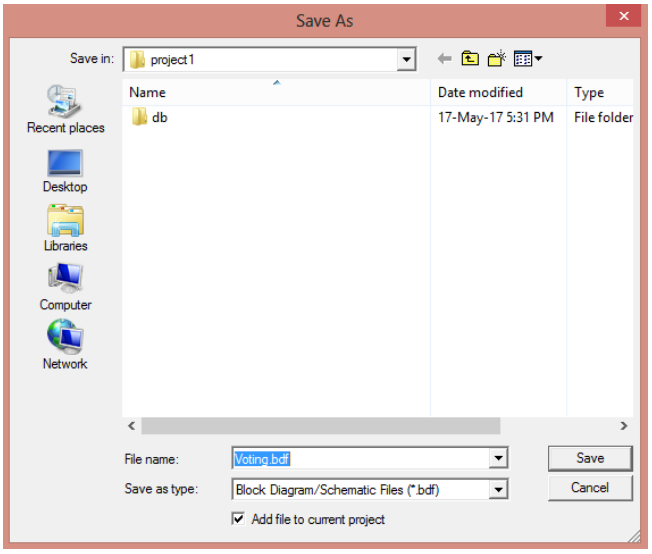


Figure 19. *Save the file.*

18. Go to Process ➥ Start and click Analysis and Synthesis. We can also simply click on the button on the menu bar. The compilation report and a pops up dialog box appear after Analysis & Synthesis compilation such shown in Fig. 20. As for this tutorial, we are not going to evaluate the report and warnings. Click OK.

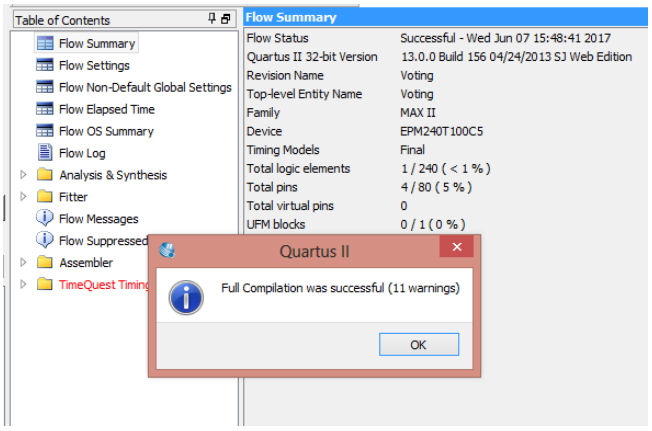


Figure 20. *Save the file.*

7. Simulation

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Acknowledgments

Thanks to Siti Nursyuhada binti Mahsahirun and Zulkifli Md. Yusof, both of Faculty of Manufacturing, Universiti Malaysia Pahang for the original idea.

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[2] *Introduction to the Quartus® II Software*. Version 10. Altera. 2010. URL: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/manual/intro_to_quartus2.pdf.

[3] *My First FPGA Design Tutorial*. Altera. July 2008. URL: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/tt/tt_my_first_fpga.pdf.