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UTM
UNIVERSITI TEKNOLOGI MALAYSIA

School of Electrical Engineering

SKEE 2742

SCHOOL OF ELECTRICAL ENGINEERING
FACULTY OF ELECTRICAL ENGINEERING
UTM JOHOR BAHRU

DIGITAL ELECTRONICS LABORATORY

TRAFFIC LIGHT SYSTEM

(STUDENT PACK)

Prepared by : **Laboratory academic coordinator**	Approved by : **Director**
Name :	Name :
Signature & Stamp :	Signature & Stamp :
Date :	Date :

1. INTRODUCTION

In this lab exercise, a 4-junction traffic light system, as shown in Figure 1 will be designed, built, simulated and verified using Quartus and CPLD (Complex Programmable Logic Device). Generally, the 4-junction traffic light system has three types of signaling (total of 10 signalings) and a two-tiers sensor (total of 8 sensors) described in Table 1. For design simplification, the yellow signal is not considered in the system, and for the arrow and pedestrian signals, no red signals are present. Besides, there is also a one-digit 7-segment display to display the countdown timer for each signaling duration. Which signaling and sensors required for each group of students depend on the specifications that will be given to them in the second week.

Table 1: Signalling and sensor

No	Type	Signaling/ Sensor	Symbol
1.	Junction without a turn signal	All direction: L_{EA} (east junction), L_{WA} (west junction)	
2.	Junction with turn signal	Right turn: L_{NR} (north junction), L_{SR} (south junction) Forward: L_{NF} (north junction), L_{SF} (south junction) Left turn: L_{NL} (north junction), L_{SL} (south junction)	
3.	Pedestrian signal	Crossing: L_{EP} (east junction), L_{WP} (west junction)	
4.	Vehicle detector sensor	First-tier: S_{N1}, S_{E1}, $S_{S1,}$ and S_{W1} Second-tier: S_{N2}, S_{E2}, $S_{S2,}$ and S_{W2}	
5.	Timer display	One digit 7-segment display	

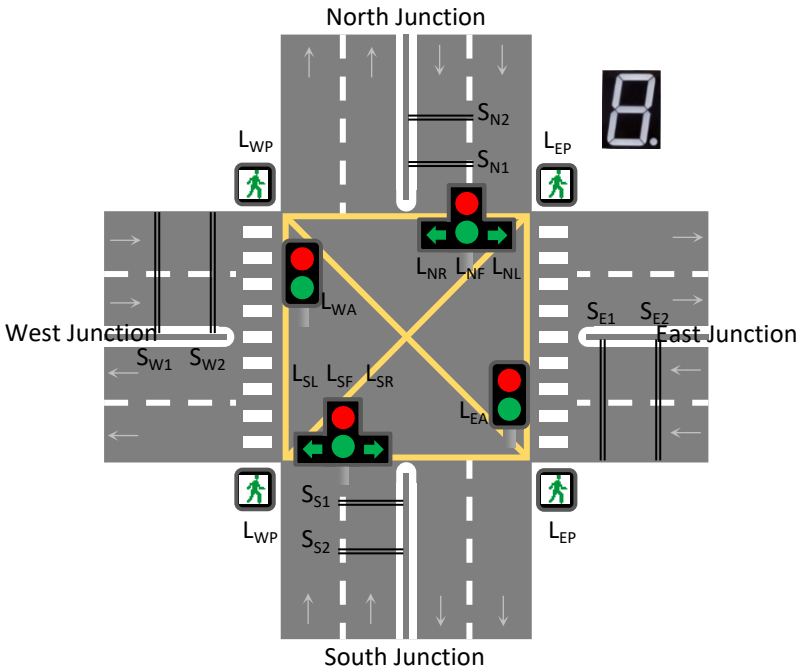

Figure 1

To design the traffic light system, refer to the circuit shown in Figure 2. There are three modules in the circuit consisting of controller, slow clock and timer circuits. The controller will control the signaling sequence, the

slow clock circuit is to reduce the CPLD high-speed clock of 50 MHz to the approximately 1 Hz clock, and the timer is to set the duration of each signaling.

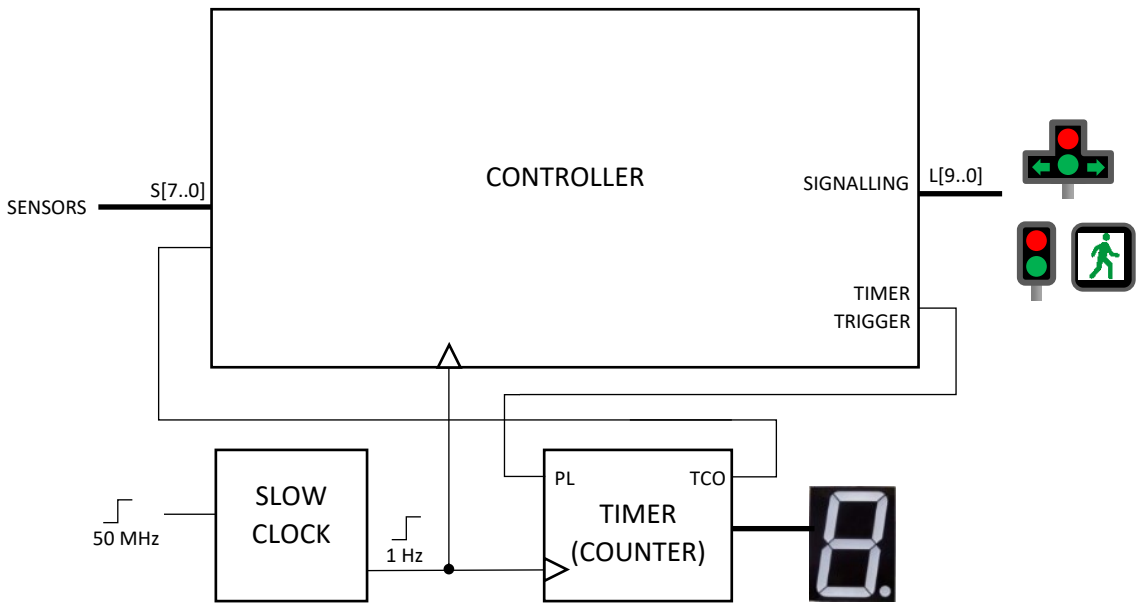

Figure 2

2. TOOLS AND EQUIPMENT

Table 2 lists the tools and equipment needed to perform the four weeks experiment.

Table 2: Tools and Equipment

No	Tool / Equipment	Remark
1.	Breadboard	Own purchase
2.	Digital Trainer	Available at Digital lab
3.	Schematic Capture Software (Multisim / KiCad / etc.)	Multisim is available at Basic Electronic lab (P04-level 3) KiCAD can be downloaded from kicad-pcb.org
4.	ICs and Electronic components	Available at Digital Lab
5.	Quartus II version 13.0sp1	Can be downloaded from http://fpgasoftware.intel.com/
6.	CPLD	Own purchased (can be purchased at Digital lab).
7.	Wire/cable	Own purchase

3. SCHEDULE

This lab takes four weeks to complete as the followings:

WEEK 1 : **2-digit decimal counter**
Circuit prototyping on a breadboard

WEEK 2 : **Traffic light controller Ver.01**
Design the given traffic light specifications using Quartus state machine editor

WEEK 3 : **Traffic light controller Ver.02**
Design the given traffic light specifications using 'one hot' method

WEEK 4 : **Traffic light system**
Program the traffic light controller Ver.02 on CPLD

4. APPLICATION NOTE

Below is the list of application notes that can be used as a guide to complete the tasks given in this lab sheet. These application notes can be downloaded from the Digital Lab website.

Table 3: Application notes

Application Note	Title
AN1	Introduction to Breadboarding
AN2	How to Draw a Schematic Diagram
AN3	Getting Started with Quartus
AN4	EPM240 Board
AN5	Finite State Machine with State Machine Editor
AN6	One Hot State Machine with Block Diagram Editor
AN11*	Serial Adder with Quartus LPM
AN12*	Serial Adder with Custom Modules

* Additional application notes which might be useful.

WEEK 1
2-DIGIT DECIMAL COUNTER

W1.1 Objectives

1. To expose the student to circuit implementation using discrete IC.
2. To familiarize students with datasheets and prototyping schematic drawings.
3. To introduce students to the implementation of prototyping using breadboards and digital trainers.

W1.2 Instruction

You are required to design and built a 1-digit decimal down counter from decimal value A to decimal value B on a breadboard (refer AN1). Values of A and B will be given before the lab session, which will be available on the lab's website. Figure W1.1 shows a general circuit of the counter, which consists of three primary circuits namely counter circuit, terminal count detector circuit, and BCD to 7-segment decoder circuit. Refer to Section 1.3 and 1.4 for the detail instructions. Note that this counter circuit is the timer circuit shown in Figure 2.

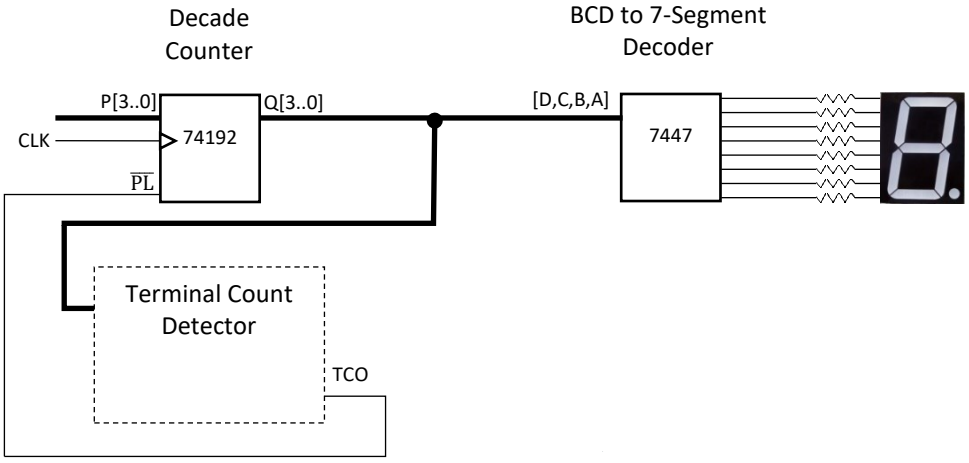

Figure W1.1

Group: _____

Name: _____

W1.3 Pre-Lab Activities

No	Task		Checked by	Marks
1	Design the terminal count detector circuit shown in Figure W1.1 using NAND gates.			/4
2	Download standard datasheets for 74192, 7447/8, 7400 and 7-Segment Display and show the evidence to the supervisor.			/2
3	Answer the following questions.			
	a) What is the maximum supply voltage for the 74LS family?	Answer:		/2
	b) What is the assumed logic value if the TTL input is not connected?	Answer:		/2
	c) Which pins must be high to enable counting for IC 74192?	Answer:		/2
	d) What is the suitable resistor value for the 7-segment display?	Answer:		/2
4	Draw the schematic diagram for the circuit shown in Figure W1.1 using schematic capture software (refer Table 2). The drawing should include labels for DC supply and I/O pin numbers as in the actual IC pin configuration (Refer AN2).			/6

** Supervisor should check whether the pre-lab items have been completed before the lab activity started by signing the right column of the above table.*

** Every group member should submit one copy of this form.*

Group: _____

W1.4 In Lab Activities

No	Task	
1	Connect a BCD to 7-segment decoder circuit using IC 7447 on a breadboard. Then, test and verify each of the circuit using a digital trainer.	
	Supervisor comments:	Supervisor name & signature:
2	Connect a counter circuit using IC 74LS192 on a breadboard to count down from 9 to 0. Then, test and verify each of the circuit using a digital trainer. Do not combine the counter circuits with the 7-segment decoder circuit yet. Instead, test the circuit as a separate module.	
	Supervisor comments:	Supervisor name & signature:
3	Connect the terminal count detector circuit designed in pre-lab on a breadboard. Then integrate the circuit with task 1 and task 2 circuits according to your circuit design and schematic drawing. Then, test and verify the overall circuit using a digital trainer.	
	Supervisor comments:	Supervisor name & signature:

** Estimated time to complete each of the above tasks is one hour. The supervisor should at least check the work at the end of every hour and comment on the progress of each task in the given column.*

**For each group, submit only one copy of this form.*

Group: _____

W1.5 Discussion

Discuss strategies and observations in completing the tasks in Section W1.4. You should also discuss the schematic diagram and the functional simulation output of your circuit. Attach the schematic diagram and the functional simulation output with this report.

W1.6 Conclusion

Statement on whether the output met the design criteria, evaluation for the effectiveness of the steps taken to complete the tasks, and if the task is not complete, explain why things did not go as expected.

**Use separate sheet if space provided for discussion and conclusion is not sufficient.*

**For each group, submit only one copy of this form.*

WEEK 2
TRAFFIC LIGHT CONTROLLER DESIGN USING STATE MACHINE EDITOR

W2.1 Objectives

1. To design state diagram based on a given specification.
2. To enter and compile a state diagram using Quartus State Machine Editor.
3. To simulate and verify the state machine.

W2.2 Instruction

Referring to Figure 2, week 2 will focus only on the design of the controller module. As shown in Figure W2.1, the slow clock and the timer circuit are disconnected from the controller, where the controller module will be simulated and verified as a separate unit. Based on the specification given to your group, performed all task described in Section W2.3 and W2.4 using Quartus (refer AN3).

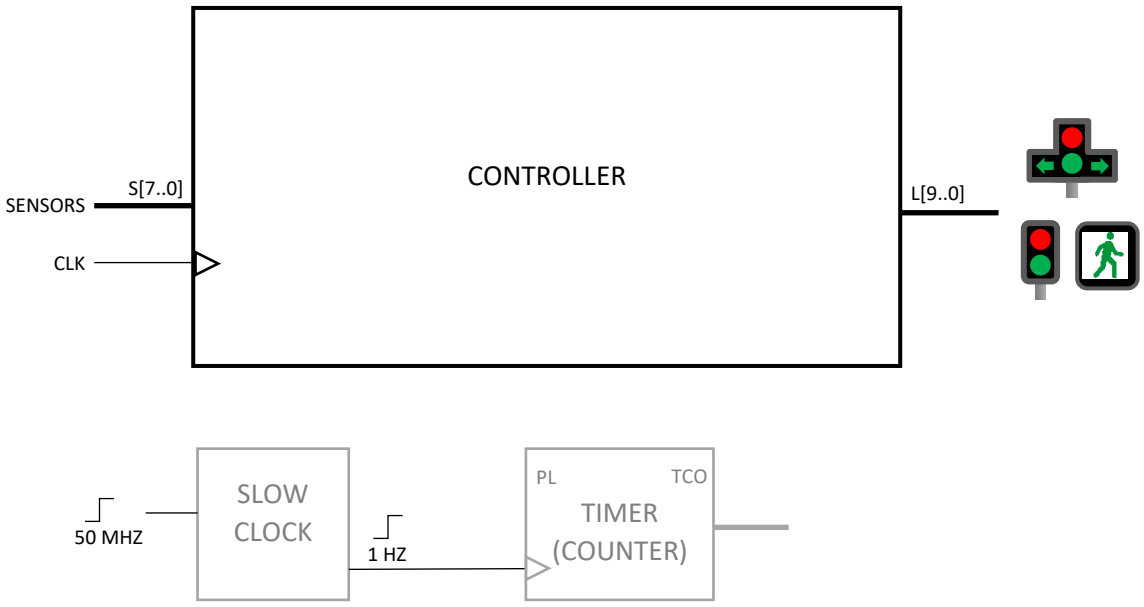

Figure W2.1

Group: _____

Name: _____

W2.3 Pre-Lab Activities

No	Task		Checked by	Marks
1	Referring to AN5, simulate the state machine example using Quartus State Machine Editor. Demo the simulation to the supervisor at the start of the lab session.			/8
2	Referring to AN5, answer the following questions:			
	a) How many states are required to implement the Moore type vending machine?	Answer:		/3
	b) Using binary state encoding, how many flip flops are required?	Answer:		/3
	c) On page 3 of the Quartus new project wizard, is it important to select the device family for state machine functional simulation?	Answer:		/3
	d) Which type of simulation is performed in the AN5?	Answer:		/3

** Supervisor should check whether the pre-lab items have been completed before the lab activity started by signing the right column of above the table.*

** Every group member should submit one copy of this form.*

Group: _____

W2.4 In Lab Activities

No	Task	
1	Design and draw a state diagram based on the given specification on A4 size paper.	
	Supervisor comments:	Supervisor name & signature:
2	Enter and compile the state diagram using Quartus State Machine Editor.	
	Supervisor comments:	Supervisor name & signature:
3	Simulate and verify the state machine.	
	Supervisor comments:	Supervisor name & signature:

**Estimated time to complete each of the above tasks is one hour. Thus, the supervisor should at least check the work at the end of every hour and comment on the progress of each task in the given column.*

**Attach all results to this lab sheet.*

**For each group, submit only one copy of this form.*

Group: _____

W2.5 Discussion

Discuss strategies and observations in completing the tasks in Section W2.4. You should also discuss the schematic diagram and the functional simulation output of your circuit. Attach the schematic diagram and the functional simulation output with this report.

W2.6 Conclusion

Statement on whether the output met the design criteria, evaluation for the effectiveness of the steps taken to complete the tasks, and if the task is not complete, explain why things did not go as expected.

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WEEK 3
TRAFFIC LIGHT CONTROLLER DESIGN VER.02

W3.1 Objectives

1. To design a traffic light controller circuit using One Hot method.
2. To build and verify a circuit using the Quartus block diagram editor.
3. To simulate and verify the integrated traffic light controller circuit and the timer circuit.

W3.2 Instruction

This week will focus on the design of the controller and timer circuits without the slow clock circuit connected. However, compared to week 2, the controller will be designed as a one-hot state machine using a block diagram editor. Design the traffic light controller with the specification given at week 2. Detail tasks are described in Section W3.3 and W3.4. Use Quartus to build, simulate and verify the circuits.

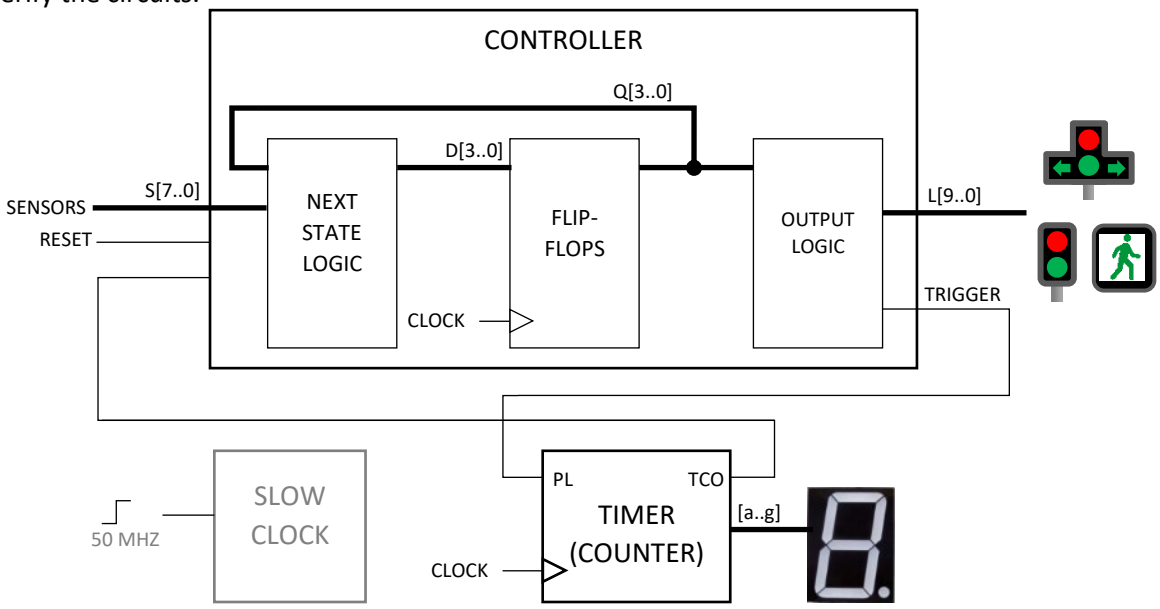

Figure W3.1

Group: _____

Name: _____

W3.3 Pre-Lab Activities

No	Task	Checked by	Marks
1	Derive the next state equation and output equation based on the week 2 state diagram (refer AN6).		/8
2	Answer the following questions:		
	a) How many flip-flops required for one hot controller with 4 states?	Answer:	/3
	b) Which pin of the down counter IC will be active when the counter reaches zero.?	Answer:	/3
	c) At any time, how many flip-flops will produce output high?	Answer:	/3
	d) In a particular one-hot design, State A is always followed by state B (unconditional transition). What is the label on the arrow from A to B?	Answer:	/3

** Supervisor should check whether the pre-lab items have been completed and correct before the lab activity started by signing the right column of the above table.*

** Every group member should submit one copy of this form.*

Group: _____

W3.4 In Lab Activities

No	Task	
1	Referring to Figure W3.1, build the timer circuit as a separate module. The module should have one clock input, one parallel load input pin (PL), one terminal count output pin (TCO) and seven output to be connected to the 7-segment display. Then, create a symbol file from the timer circuit. Note that the design is similar to the week 1 timer circuit but without the terminal count circuit.	
	Supervisor comments:	Supervisor name & signature:
2	Based on the next state and output equations derived from the pre-lab, build, simulate and verify the traffic light controller circuit. Finally, create a symbol file from the controller circuit.	
	Supervisor comments:	Supervisor name & signature:
3	Integrate the traffic light controller circuit with the timer circuit. Then, simulate and verify the overall circuit.	
	Supervisor comments:	Supervisor name & signature:

**Estimated time to complete each of the above tasks is one hour. Thus, the supervisor should at least check the work at the end of every hour and comment on the progress of each task in the given column.*

**Attach all results to this lab sheet.*

**For each group, submit only one copy of this form.*

Group: _____

W3.5 Discussion

Discuss strategies and observations in completing the tasks in Section W3.4. You should also discuss the schematic diagram and the functional simulation output of your circuit. Attach the schematic diagram and the functional simulation output with this report.

W3.6 Conclusion

Statement on whether the output met the design criteria, evaluation for the effectiveness of the steps taken to complete the tasks, and if the task is not complete, explain why things did not go as expected.

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WEEK 4
TRAFFIC LIGHT SYSTEM

W4.1 Objectives

1. To build a circuit using Quartus text editor.
2. To verify a slow clock circuit using CPLD with LED.
3. To complete the traffic light system.

W4.2 Instruction

Week 4 is to complete the whole circuit, as shown in Figure W4.1 and program the circuit to CPLD (refer to AN4). Then, the completed CPLD based traffic light system will be tested on a traffic light board available in the lab. Detail tasks are described in Section W4.3 and W4.4.

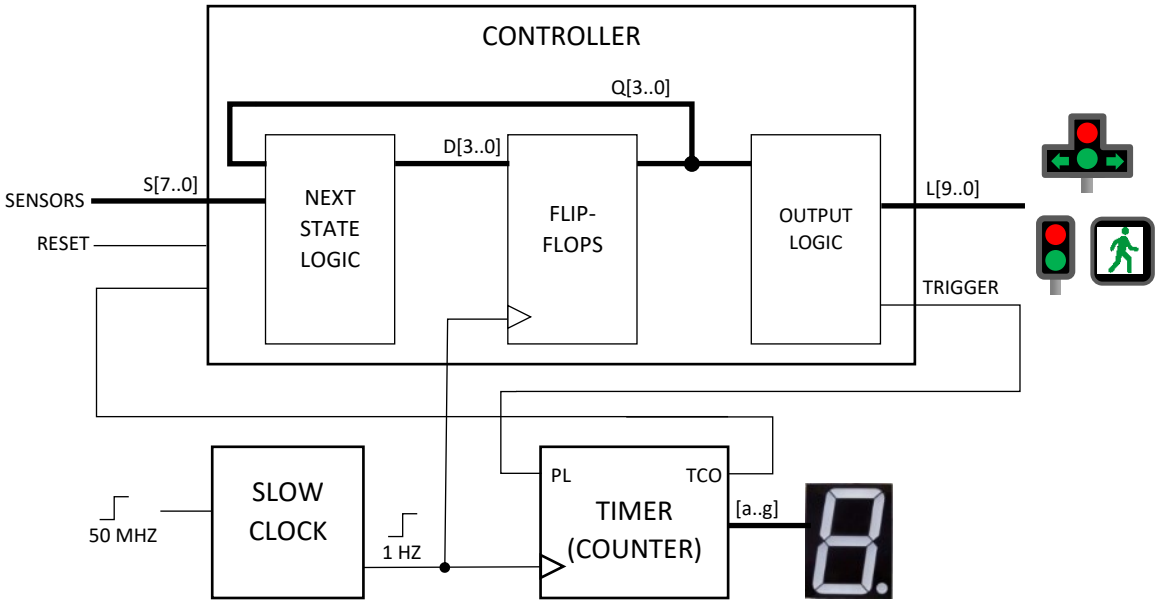

Figure W4.1

Group: _____

Name: _____

W4.3 Pre-Lab Activities

No	Task		Checked by	Marks
1	Referring to AN4, build the LED blinker using Quartus text editor and program it to CPLD to demonstrate the 1 Hz clock. Demo the blinker to the supervisor at the start of the lab session.			/8
2	Referring to AN4, answer the following question:			
	a) What is the operating voltage of the CPLD?	Answer:		/3
	b) What is the frequency of the slow clock?	Answer:		/3
	c) To get the 1 Hz cycle at the slow clock output, what is the divisor?	Answer:		/3
	d) What is the pin number for the CPLD 50MHz clock?	Answer:		/3

** Supervisor should check whether the pre-lab items have been completed before the lab activity started by signing the right column of the above table.*

** Every group member should submit one copy of this form.*

Group: _____

W4.4 In Lab Activities

No	Task	
1	Integrate the slow clock (built from the pre-lab) and the timer module (built from week 3). Since the controller module is not present at this stage, connect the timer output TCO to the input PL. Then, program the module to CPLD and verify the output by connecting the CPLD output to a 7-segment display on a breadboard.	
	Supervisor comments:	Supervisor name & signature:
2	Integrate the traffic light controller ver.02 with the circuit in task 1. Next, program the integrated module to CPLD.	
	Supervisor comments:	Supervisor name & signature:
3	Demo the Traffic Light System on the traffic light board.	
	Supervisor comments:	Supervisor name & signature:

**Estimated time to complete each of the above tasks is one hour. Thus, the supervisor should at least check the work at the end of every hour and comment on the progress of each task in the given column.*

**Attach all results to this lab sheet.*

**For each group, submit only one copy of this form.*

Group: _____

W4.5 Discussion

Discuss strategies and observations in completing the tasks in Section W4.4. You should also discuss the schematic diagram and the functional simulation output of your circuit. Attach the schematic diagram and the functional simulation output with this report.

W4.6 Conclusion

Statement on whether the output met the design criteria, evaluation for the effectiveness of the steps taken to complete the tasks, and if the task is not complete, explain why things did not go as expected.

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