NAME: …… GROUP NAME: ……

PRE-LAB WEEK 1
2-DIGIT DECIMAL COUNTER

W1.1 Objectives

1. To expose student to circuit implementation using discrete IC.
2. To familiarize students with data sheets and prototyping schematic drawings.
3. To introduce students to the implementation of prototyping using breadboard and digital trainers.

W1.3 Pre-Lab Activities

No	Task		Checked by	Marks
1	Design the terminal count detector circuit shown in Figure W1.1 using NAND gate.			/4
2	Download standard datasheets for 74192, 7447/8, 7400 and 7-Segment Display and show the evidence to the supervisor.			/2
3	Answer the following questions.			
	a) What is the maximum supply voltage for the 74LS family?	Answer:		/2
	b) What is the assumed logic value if the TTL input is not connected?	Answer:		/2
	c) Which pins must be high to enable counting for IC 74192?	Answer:		/2
	d) What is the suitable resistor value for the 7-segment display?	Answer:		/2
4	Draw the schematic diagram for the circuit shown in Figure W1.1 using schematic capture software (refer Table 2). The drawing should include labels for DC supply and I/O pin numbers as in the actual IC pin configuration (Refer AN2).			/6
TOTAL				**/20**

** Supervisor should check whether the pre-lab items have been completed before the lab activity started by signing the right column of above the table.*

NAME: …… GROUP NAME: ……

PRE-LAB WEEK 2
TRAFFIC LIGHT CONTROLLER DESIGN USING STATE MACHINE EDITOR

W2.1 Objectives

1. To design state diagram based on a given specification.
2. To enter and compile a state diagram using Quartus State Machine Editor.
3. To simulate and verify the state machine.

W2.3 Pre-Lab Activities

No	Task		Checked by	Marks
1	Referring to AN5, simulate the state machine example using Quartus State Machine Editor. Demo the simulation to the supervisor at the start of the lab session.			/8
2	Referring to AN5, answer the following questions:			
	a) How many states are required to implement the Moore type vending machine?	Answer:		/3
	b) Using binary state encoding, how many flip flops are required?	Answer:		/3
	c) In page 3 of Quartus new project wizard, is it important to select the device family for state machine	Answer:		/3
	d) Which type of simulation is performed in the AN5?	Answer:		/3
	TOTAL			

** Supervisor should check whether the pre-lab items have been completed before the lab activity started by signing the right column of above the table.*

NAME: …… GROUP NAME: ……

PRE-LAB WEEK 3
TRAFFIC LIGHT CONTROLLER DESIGN VER.02

W3.1 Objectives

1. To design a traffic light controller circuit using One Hot method.
2. To build and verify a circuit using Quartus block diagram editor.
3. To simulate and verify the integrated traffic light controller circuit and the timer circuit.

W3.3 Pre-Lab Activities

No	Task	Checked by	Marks
1	Derive next state equation and output equation based on week 2 state diagram (refer AN6).		/8
2	Answer the following questions:		
	a) How many flip-flops required for one hot controller with 4 states?	Answer:	/3
	b) Which pin of the down counter IC will be active when the counter reach zero.?	Answer:	/3
	c) At any time, how many flip-flops will produce output high?	Answer:	/3
	d) In a particular one hot design, State A is always followed by state B (unconditional transition). What is the label on the arrow from A to B?	Answer:	/3
	TOTAL		

** Supervisor should check whether the pre-lab items have been completed and correct before the lab activity started by signing the right column of above the table.*

NAME: …… GROUP NAME: ……

PRE-LAB WEEK 4 TRAFFIC LIGHT SYSTEM

W4.1 Objectives

1. To build a circuit using Quartus text editor.
2. To verify a slow clock circuit using CPLD with LED.
3. To complete the traffic light system.

W4.3 Pre-Lab Activities

No	Task		Checked by	Marks
1	Referring to AN4, build the LED blinker using Quartus text editor and program it to CPLD to demonstrate the 1 Hz clock. Demo the blinker to the supervisor at the start of the lab session.			/8
2	Referring to AN4, answer the following question:			
	a) What is the operating voltage of the CPLD?	Answer:		/3
	b) What is the frequency of the slow clock?	Answer:		/3
	c) To get the 1 Hz cycle at the slow clock output, what is the	Answer:		/3
	d) What is the pin number for the CPLD 50MHz clock?	Answer:		/3
	TOTAL			